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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,668	04/22/2004	Douglas C. Burger	888.003US1	6831

21186 7590 05/24/2007

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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

MAIL DATE	DELIVERY MODE
05/24/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,668	BURGER ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/7/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 18-36 are pending. Examiner acknowledges Applicant's election of Group II from the previous restriction. Claims 1-17 cancelled as per Applicant's request. Claims 28 and 31-36 amended as per Applicants request.

Claim Objections

2. Claim 19 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 19 further limits the node disclosed in Claim 18, however, Claim 19 fails to further limit the method of Claim 18, as it introduces no new steps, nor does it further limit any of the disclosed steps, and as a result does not further limit the subject matter of the independent claim upon which it is based.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 18-20, 24-29, and 31-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Requa et al. ("The Piecewise Data Flow Architecture: Architectural Concepts", herein Requa).

5. As per Claim 18, Requa teaches: A method, comprising:

partitioning a program into a plurality of groups of instructions (Page 426, first column, second paragraph, instructions are grouped into blocks);

assigning a group of instructions selected from the plurality of groups of instructions to a plurality of interconnected preselected computation nodes (Page 426, first column, second paragraph, the blocks are sent to processors);

loading the group of instructions to the plurality of interconnected preselected computation nodes (Page 426, first column, second paragraph, also see Page 433, "The PDF Block Processor"); and

executing the group of instructions as each one of the instructions in the group of instructions receives all necessary associated operands for execution (Page 433, first column, third paragraph, an instruction waits for input operands, then is executed).

6. As per Claim 19, Requa teaches: The method of claim 18, wherein at least one computation node included in the plurality of interconnected preselected computation nodes has at least one input port capable of being coupled to at least one preselected first other computation node included in the plurality of interconnected preselected computation nodes (Figure 1),

the input port to receive input data (Page 427, second column, Paragraph 2 (any consumer can receive any data), also see Page 433, The PDF Block Processor (herein referred to as PDF for the remainder of this claim, as this section will be referenced several times). Additionally, one would recognize a processor/execution unit inherently requires an input port to receive data),

a first store coupled to the at least one input port to store the input data (PDF, paragraph 1, input operands are stored in registers),

a second store coupled to an instruction sequencer, the second store to receive and store the at least one instruction (PDF, Paragraph 1, the instruction issue section holds instructions prior to execution),

an instruction wakeup unit to match the input data to the at least one instruction (PDF, paragraph 1, the operand source fields are modified as data comes in), at least one execution unit to execute the at least one instruction using the input data to produce output data (PDF, paragraph 1, the instructions are executed after receiving inputs),

at least one output port capable of being coupled to at least one second other preselected computation node included in the plurality of interconnected preselected computation nodes (Figure 1 and Page 427, see below), and

a router to direct the output data from the at least one output port to the at least one preselected second other computation node (Page 427, second column, paragraph 2. Any consumer can receive any data from the interconnection network, thus all processors are capable of sending data to any other processor).

7. As per Claim 20, Requa teaches: The method of claim 18, wherein at least one of the plurality of groups of instructions is a basic block (Page 426, first column third paragraph).

8. As per Claim 24, Requa teaches: The method of claim 18, wherein loading the group of instructions to the plurality of interconnected preselected computation nodes includes:

sending at least two instructions selected from the group of instructions from an instruction sequencer to a selected computation node included in the plurality of interconnected preselected computation nodes for storage in a store (Page 426, Column 1, Paragraph 2, each instruction is sent out to a selected processor/functional unit/node).

9. As per Claim 25, Requa teaches: The method of claim 18, wherein executing the group of instructions as each one of the instructions in the group of instructions receives all necessary associated operands for execution includes:

matching at least one instruction selected from the group of instructions with at least one operand received from an other computation node included in the plurality of interconnected preselected computation nodes (Page 427, second column, second paragraph, where any consumer (processor) can receive any data, and instructions waiting to execute wait for results from the processor before executing).

10. As per Claim 26, Requa teaches: The method of claim 18, wherein loading the group of instructions to the plurality of interconnected preselected computation nodes includes:

Sending a first set of instructions selected from a first group of instructions selected from the plurality of groups of instructions from an instruction sequencer to the plurality of interconnected preselected computation nodes for storage in a first frame included in a first computation node included in the plurality of interconnected preselected computation nodes (Page 433, PDF, paragraph 1, the instruction issue section is a buffer where instructions wait to be executed); and

sending a second set of instructions selected from the first group of instructions from the instruction sequencer to the plurality of interconnected preselected computation nodes for storage in a second frame included in the first computation node (Page 433, PDF, paragraph 1, the instruction issue section is a buffer where instructions wait to be executed).

11. As per Claim 27, Requa teaches: The method of claim 18, wherein assigning a group of instructions selected from the plurality of groups of instructions to a plurality of interconnected preselected computation nodes includes:

assigning a first group of instructions to a first set of frames included in the plurality of interconnected preselected computation nodes (Page 433, PDF, paragraph 1, the instruction issue section is a buffer where instructions wait to be executed);

assigning a second group of instructions to a second set of frames included in the plurality of interconnected preselected computation nodes (Page 433, PDF, paragraph 1, the instruction issue section is a buffer where instructions wait to be executed), wherein the first group and the second group of instructions are capable of concurrent execution (Abstract), and wherein at least one output datum associated with the first group of instructions is written to a register file and passed directly to the second group of instructions for use as an input datum by the second group of instructions (Page 430, first column, second paragraph, when an instruction completes, the results are written to a register, which is then read by the dependent instruction).

12. As per Claim 28, Requa teaches: An article comprising a machine-accessible medium having associated information, wherein the information, when accessed, results in a machine performing:

partitioning a program into a plurality of groups of instructions (Page 426, first column, second paragraph, instructions are grouped into blocks);

assigning a group of instructions selected from the plurality of groups of instructions to a plurality of interconnected preselected computation nodes (Page 426, first column, second paragraph, the blocks are sent to processors);

loading the group of instructions to the plurality of interconnected preselected computation nodes (Page 426, first column, second paragraph, also see Page 433, "The PDF Block Processor"); and

executing the group of instructions as each one of the instructions in the group of instructions receives all necessary associated operands for execution (Page 433, first column, third paragraph, an instruction waits for input operands, then is executed).

13. As per Claim 29, Requa teaches: The article of claim 28, wherein partitioning the program into the plurality of groups of instructions is performed by a compiler (Page 429, first column, "PDF Architecture").

14. As per Claim 31, Requa teaches: The article of claim 28, wherein the machine-accessible medium further includes information, which when accessed by the machine, results in the machine performing:

Statically assigning all of the plurality of groups of instructions for execution (Page 432, see Figure 8, and column 1, paragraph 2).

15. As per Claim 32, Requa teaches: The article of claim 31, wherein the machine-accessible medium further includes information, which when accessed by the machine, results in the machine performing:

dynamically issuing one or more instructions from at least one of the plurality of groups of instructions for execution (Page 426, second column, third paragraph. Instructions are issued as dependent operands come in).

16. As per Claim 33, Requa teaches: The article of claim 28, wherein the machine-accessible medium further includes information, which when accessed by the machine, results in the machine performing:

generating a wakeup token to reserve an output data channel to connect selected computation nodes included in the plurality of interconnected preselected computation nodes (Page 427, section column, second paragraph).

17. As per Claim 34, Requa teaches: The article of claim 28, wherein the machine-accessible medium further includes information, which when accessed by the machine, results in the machine performing:

detecting execution termination of the group of instructions including an output having architecturally visible data (Page 433, second column first paragraph, a flag is set when an execution is done, also see Page 430, second paragraph); and

committing the architecturally visible data to a register file (Page 430, second paragraph).

18. As per Claim 35, Requa teaches: The article of claim 28, wherein the machine-accessible medium further includes information, which when accessed by the machine, results in the machine performing:

detecting execution termination of the group of instructions including an output having architecturally visible data (Page 433, second column first paragraph, a flag is set when an execution is done, also see Page 430, second paragraph); and

committing the architecturally visible data to a memory (Page 430, second paragraph).

19. As per Claim 36, Requa teaches: The article of claim 28, wherein the machine-accessible medium further includes information, which when accessed by the machine, results in the machine performing:

routing an output datum arising from executing the group of instructions to a consumer node included in the plurality of interconnected preselected computation nodes, wherein the address of the consumer node is included in a token associated with at least one instruction included in the group of instructions (Page 429, second column, second paragraph).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Requa, in view of Official Notice.

22. As per Claim 21, Requa teaches: The method of claim 18, but fails to teach:

wherein at least one of the plurality of groups of instructions is a hyperblock.

Requa teaches of a system which uses basic blocks, but does not teach that the groups may be hyperblocks. However, Examiner is taking Official Notice that one of ordinary skill in the art would be capable and motivated to use hyperblocks in lieu of basic blocks, to take advantage of the ability to have multiple exits from a block (While Applicant has not provided a definition of a hyperblock, Examiner has found it to represent a block with one entrance and potentially (but not necessarily) more than one exit).

23. As per Claim 22, Requa teaches: The method of claim 18, but fails to teach: wherein at least one of the plurality of groups of instructions is a superblock.

Requa teaches of a system which uses basic blocks, but does not teach that the groups may be superblocks. However, Examiner is taking Official Notice that one of ordinary skill in the art would be capable and motivated to use superblocks in lieu of basic blocks, to take advantage of the ability to have multiple exits from a block (While Applicant has not provided a definition of a superblock, Examiner has found it to represent a block with one entrance and potentially (but not necessarily) more than one exit, however, Examiner is unclear how a superblock is different from a hyperblock).

24. Claims 23 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Requa, in view of Fisher.

25. As per Claim 23, Requa teaches: The method of claim 18, but fails to teach:

wherein at least one of the plurality of groups of instructions is an instruction trace constructed by a hardware trace construction unit at run time.

While Requa teaches the method as disclosed in Claim 18, Requa does not teach about traces, or a trace construction unit to construct such a trace. However, Fisher teaches of Trace Scheduling, where the basic blocks used by Requa are compacted, and instead use traces (Page 462, Section D). The advantage to this compaction method using traces allows for more efficient parallel code, done in a manner far more efficient than previous methods (Abstract). Given this advantage, one of ordinary skill in the art would have been motivated to use these traces in place of the basic blocks as taught by Requa to further increase the efficiency of the system.

26. As per Claim 30, Requa teaches: The article of claim 28, but fails to teach:

wherein partitioning the program into the plurality of groups of instructions is performed by a run-time trace mapper.

While Requa teaches the article as disclosed in Claim 28, Requea does not teach that the partitioning of the program is done by a trace mapper. However, Fisher teaches of Trace Scheduling, where the basic blocks used by Requa are compacted, and instead use traces (Page 462, Section D), created and optimized by a scheduler (Page 482, second column, second paragraph). The advantage to this compaction method using traces allows for more efficient parallel code, done in a manner far more efficient than previous methods (Abstract). Given this advantage, one of ordinary skill in

the art would have been motivated to use these traces in place of the basic blocks as taught by Requa to further increase the efficiency of the system.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

28. Papadopoulous et al. (USPN 5,241,635) teaches a token based machine using frames.

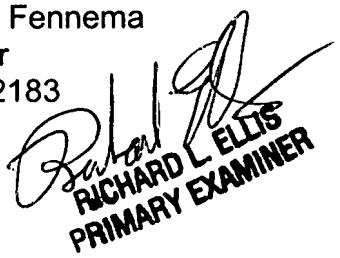
29. Dennis (USPN 4,814,978) teaches a system of partitioning instructions to execute in parallel.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183



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